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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,327	03/30/2004	Woon-Sik Suh	8729-231 (SS-20446-US)	5102

22150 7590 01/12/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
WENDELL, ANDREW	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,327	SUH ET AL.	
	Examiner	Art Unit	
	Andrew Wendell	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5-6, 11, 21, 25-26, 35-36, 40, and 44-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Funk et al. (US Pat# 6,026,119).

Regarding claim 1, Funk et al. wireless packet data communication modem teaches a signal modulator/demodulator 409 and 417 (Fig. 4) having a digital signal processor (Col. 2 lines 44-53) for effecting radio communications; and an application processor having a central processing unit 421 (Fig. 4) and a master controller 111

(Fig. 4) for controlling via a common bus a plurality of peripherals 425 (Fig. 4) including an interface with the signal modulator/demodulator 409 and 417 (Fig. 4).

Regarding claim 5, Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 6, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 21, Funk et al. teaches a central processing unit 421(Fig. 4) for processing data received from a plurality of peripherals 101 and 425 (Fig. 4); and a master controller 111 (Fig. 4) for controlling via a common bus the plurality of peripherals 101 (Fig. 4) and for interfacing with a signal modulator/demodulator (modem) 402 and 406 (Fig. 4) via the common bus.

Regarding claim 25, Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 26, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 31, Funk et al. teaches a central processing unit 421 (Fig. 4) for processing data received from a plurality of peripherals 101 and 425 (Fig. 4); and a master controller for controlling via a first bus the plurality of peripherals 425 (Fig. 4) and for interfacing with a signal modulator/demodulator 409 and 417 (Fig. 4) via a second bus.

Regarding claim 35, Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 36, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 40, Funk et al. teaches controlling via a common bus in the master controller 421 (Fig. 4) a plurality of peripherals 101 and 425 (Fig. 4); and interfacing with the signal modulator/demodulator 409 and 417 (Fig. 4) via the common bus.

Regarding claim 44, Funk et al. teaches wherein the step of controlling includes issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 45, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 7, 11-12, 14-16, 18, 22-23, 27, 32-33, 37, 41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152).

Regarding claim 2, Funk et al. wireless packet data communication modem teaches the limitations in claim 1. Funk et al. fails to teach about a memory shared by the modem and the AP is controlled via the interface.

Gibbs et al. wireless trickle sync device teaches about a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the AP 40 (Fig. 1) is controlled via the interface.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a memory shared by the modem and the AP is controlled via the interface as taught by Gibbs et al. into Funk et al. circuit in order to reduce power consumption (Section 0002).

Regarding claim 7, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Regarding claim 11, Funk et al. teaches a signal modulator/demodulator 409 and 417 (Fig. 4) having a digital signal processor (Col. 2 lines 44-53) for effecting radio communications; and an application processor having a central processing unit 421 (Fig. 4) and a master controller 111 (Fig. 4) for controlling via a first bus at least one peripheral 101 (Fig. 4) Funk et al. fails to teach via a second bus a memory shared by the modem and the AP.

Gibbs et al. wireless trickle sync device teaches a second bus a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to reduce power consumption (Section 0002).

Regarding claim 12, the combination including Gibbs et al. teaches wherein the master controller further controls via the second bus a flash memory (Section 0013).

Regarding claim 14, the combination including Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a packetized command commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the common bus 430, 432, and 434 (Fig. 4), the packetized command includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 15, the combination including Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of command (Col. 7 lines 48-54).

Regarding claim 16, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Regarding claim 18, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 22, the combination including Gibbs et al. teaches about a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the AP 40 (Fig. 1).

Regarding claim 23, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 27, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Regarding claim 32, the combination including Gibbs et al. teaches about a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the AP 40 (Fig. 1).

Regarding claim 33, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 37, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

Regarding claim 41, the combination including Gibbs et al. teaches about interfacing a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the AP 40 (Fig. 1).

Regarding claim 46, the combination including Gibbs et al. teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the AP 40 (Fig. 1).

5. Claims 3 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119).

Regarding claim 3, Funk et al. wireless packet data communication modem teaches the limitations in claims 1 and 2. Funk et al. fails to teach about shared memory of being SDRAM.

It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM

memory into Funk et al. memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

Regarding claim 42, it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

6. Claims 4, 24, 34, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 4, Funk et al. wireless packet data communication modem teaches the limitations in claim 1 and wherein the plurality of peripherals include at least one of an a display 425 (Fig. 4). Funk et al. fails to teach a plurality of peripherals include at least one of an image capture module and a flash memory.

Wilska et al. device for personal communications teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of peripherals include at least one of an image capture module and a flash memory as taught by Wilska et al. into Funk et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

Regarding claim 24, Wilska et al. teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Regarding claim 34, Wilska et al. teaches wherein the step of controlling includes controlling at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Regarding claim 43, Wilska et al. teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

7. Claims 8-9, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Watanabe et al. (US Pat# 6,378,102).

Regarding claim 8, Funk et al. Funk et al. wireless packet data communication modem teaches the limitations in claims 1 and 3. Funk et al. fails to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into Funk et al. circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 9, the combination including Watanabe et al. teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 29, the combination including Watanabe et al. teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 47, the combination including Watanabe et al. teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

8. Claims 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Fueki (US Pat Appl# 2002/0166058).

Regarding claim 10, Funk et al. wireless packet data communication modem teaches the limitations in claims 1 and 3. Funk et al. fails to teach about a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into Funk et al. circuit in order to increase security (section 0015).

Regarding claim 30, the combination including Fueki teaches wherein the memory includes a protection circuit for receiving address data from an external devices

and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claim 11 above, and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 13, the combination of Funk et al. in view of Gibbs et al. teaches the limitations in claim 11. Both Funk et al. and Wilska et al. fail to teach an image capture module.

Wilska et al. device for personal communications teaches wherein the at least one peripheral is an image capture module 14 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate an image capture module as taught by Wilska et al. into a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

10. Claim 17, 19, 28, and 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 11, 14, and 16 above, and further in view of Watanabe et al. (US Pat# 6,378,102).

Regarding claim 17, the combination of Funk et al. in view of Gibbs et al. teaches the limitations in claims 11, 14, and 16. Funk et al. and Gibbs et al. both fail to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 19, the combination including Watanabe et al. teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 28, the combination including Watanabe et al. teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 38, the combination including Watanabe et al. teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 39, the combination including Watanabe et al. teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

11. Claims 20 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 11 and 18 above, and further in view of Fueki (US Pat Appl# 2002/0166058).

Regarding claim 20, the combination of Funk et al. in view of Gibbs et al. teaches the limitations in claims 11 and 18. Funk et al. and Gibbs et al. both fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the AP as taught by Gibbs et al. into Funk et al. circuit in order to increase security (section 0015).

Regarding claim 48, the combination including Fueki teaches receiving address data from the external devices at the shared memory and generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Souissi discloses an apparatus for software configurable wireless modem adaptable for multiple modes of operation. Gupta et al. discloses power management for nodes coupled to a communication link. Whitridge et al. discloses a telecommunications adapter providing non-repudiable communications log and supplemental power for a portable programmable device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz can be reached on 571-272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Wendell

Patent Examiner

Date: 12/30/2005

DUC NGUYEN
PRIMARY EXAMINER

ASW